REMARKS

Claims 1-25 remain pending in the instant application. Claims 1-25 presently stand rejected. Claims 1-3, 8, 9, 13-15, 21, and 23 are amended herein. Claim 26 is newly presented. Entry of this amendment and reconsideration of the pending claims are respectfully requested.

Specification

Applicants have corrected a minor error in the specification by striking the word "receive" from paragraph [0020].

Claim Rejections – 35 U.S.C. § 102

Claims 1, 16, and 21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Vasic et al. (US 6,691,263).

A claim is anticipated only if each and every element of the claim is found in a single reference. M.P.E.P § 2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628 (Fed. Cir. 1987)). "The identical invention must be shown in as complete detail as is contained in the claim." M.P.E.P. § 2131 (citing *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226 (Fed. Cir. 1989)).

Independent Claim 16

The Office Action rejection of independent claim 16 quotes the language of claim 15 and gives the same rejection as is presented for claim 15. So that Applicants have a full and fair opportunity to respond to any potential rejection of independent claim 16, Applicants respectfully request that the Examiner present grounds for any such rejection of claim 16 in a new non-final office action.

Independent Claim 1 and 21

Amended independent claim 1 now recites, in pertinent part,

> **a plurality of processing elements** operating based on **associative processing**, the plurality of processing elements coupled to perform operations in **word-parallel, bit-serial format**, wherein the plurality of processing elements are further coupled to iteratively decode a received

codeword using a bit reliability value such that **for each iteration, the bit reliability value is updated based on a comparison using a threshold value** based on a plurality of threshold values that are updated during the iterative decoding, each processing element in the plurality of processing elements further including:

a memory unit for storing data, wherein the data stored within the memory unit is identified based on memory content rather than an address; and

a processing logic unit for comparing the bit reliability value with the threshold value.

Applicants respectfully submit that Vasic fails to disclose a plurality of processing elements operating based on associative processing and performing operations in word-parallel, bit-serial format. Additionally, Applicants submits that Vasic fails to disclose a memory unit where stored data is identified based on memory content rather than an address.

First, Vasic is directed towards an iterative decoding system that updates bit reliabilities. *Vasic*, Abstract. However, **Vasic fails to disclose a plurality of processing elements updating bit reliability values**. The Office Action cites Vasic col. 7, lines 26-43 in support of the rejection, but this segment of Vasic only discloses one processor – MLSD processor 103. *Office Action 12/22/2009*, p. 2. Even if Iterative Decoder 104 is considered a processing element, it is not a processing element that updates bit reliability values because its bit reliabilities are updated before reaching Iterative Decoder 104. *See Vasic*, col. 12, lines 43-47 (showing converting updated bit reliability values occurs in MAPM module 205, which is in MLSD processor 103). Therefore, since Vasic only **discloses one processor** that could process data to update bit reliabilities, it fails to disclose **a plurality of processing** elements processing data to update bit reliability values.

Similarly, Vasic fails to disclose a plurality of processing elements operating based on **associative processing** and performing operations in **word-parallel, bit-serial format**. Vasic col. 7, lines 26-43 does not disclose operating based on associative processing or performing operation in word-parallel, bit-serial format. Therefore, **Vasic fails to disclose a plurality of processing elements operating based on associative processing and performing operations in word-parallel, bit-serial format**.

Finally, **Vasic fails to disclose a memory unit where stored data is identified based on memory content rather than an address**. The Office Action cites Vasic col. 7, lines 26-43 in support of the rejection; however, this segment of Vasic fails to disclose a memory unit, much less a memory unit identifying stored data based on memory content rather than identifying the data based on an address. *Office Action 12/22/2009*, p. 2. Consequently, Vasic fails to disclose a memory unit where stored data is identified based on memory content rather than an address.

Therefore, Vasic fails to disclose each and every element of claim 1, as required under M.P.E.P. § 2131. Independent claim 21 includes similar novel elements as independent claim 1. Accordingly, withdrawal of the instant §102 rejections of claims 1 and 21 is requested.

Claim Rejections – 35 U.S.C. § 103

Claims 2-4, 10-15, and 22-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Vasic et al. in view of Hocevar (US 7,139,959).

Claims 5-6 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Vasic et al. and Hocevar in view of Lee (US 6,421,804).

Claims 7-9, 18, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Vasic et al., Hocevar and Lee in view of Yu et al. (US 7,137,060).

When combining prior art elements to establish a prima facie case of obviousness, the MPEP requires a factual finding "*…that the prior art include* ***each*** *element claimed….*" M.P.E.P. § 2143 (A)(1). "All words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03.

The dependent claims are nonobvious over the prior art of record for at least the same reasons as discussed above in connection with their respective independent claims, in addition to adding further limitations of their own. Accordingly, Applicants respectfully request that the instant § 103 rejections of the dependent claims be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, it is believed that the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative at (206) 292-8600 if the Examiner believes that an interview might be useful for any reason.

CHARGE DEPOSIT ACCOUNT

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a). Any fees required therefore are hereby authorized to be charged to Deposit Account No. 02-2666. Please credit any overpayment to the same deposit account.

Respectfully submitted,
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

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/Cory G. Claassen/

Cory G. Claassen
Reg. No. 50,296
Phone: (206) 292-8600

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040